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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,512	01/23/2004	Christopher Lapkowski	CA920030044US1	7220

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EXAMINER	
VU, TUAN A	
ART UNIT	**PAPER NUMBER**
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/763,512	LAPKOWSKI, CHRISTOPHER	
	Examiner	Art Unit	
	Tuan A. Vu	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/23/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed 1/23/2004.

Claims 1-23 have been submitted for examination.

Specification

2. The disclosure is objected to because of the following informalities: The use of phraseology like 'can be associated' in regard to spills instructions seem unclear as to the context implicated by the act of associating 2 entities. The language used does not make it explicit as to what is at the end points of the association possibility being conveyed by the phrase 'can be associated'. There is lack of definition as to what exactly associating a spill instruction means or as to how it is implemented.

3. The specification mentions about an architecture having a set of primary and secondary registers as illustrated in Fig. 2; and describes this using a phrase such as 'parallel register architecture'. For one skill in the art, the illustration of 2 rows of registers without further hardware specification in regard to a particular hardware-based architecture cannot achieve what is commonly accepted meaning for 'architecture' which entails much more hardware details. The Specifications does not provide further details as how setting 2 registers in a Figure can make the registers an 'architecture' in the true meaning expected of it. It appears that the language used so to automatically raise the registers to the state of a 'parallel register architecture' is inadequate if not improper, absent description needed to establish that the registers are only part of a more elaborate architecture, the architectural details about which apparently not disclosed. The above phraseology will be treated as a setting wherein registers

are disposed in columns or in plurality such that one register set are more *primary* than another. Correction to the claim language to this effect is also recommended.

Appropriate correction is required.

Claim Objections

4. Claims 1, 9, 16, 20 are objected to because of the following informalities:

The *architecture* limitation recited in the phrase 'parallel register architecture' does not provide sufficient teaching as to how the parallel nature of using/disposing registers as claimed can render the outset as being a 'parallel register architecture' because registers (even as disposed in parallel columns) cannot be themselves represent a whole computer architecture lacking sufficient teaching from the Specifications to corroborate such commonly-known concept; as set forth above. As set forth in the Specifications Objections based on common knowledge about computer useful arts, one would not be able to construe the combination of 'parallel register' concept and the term 'architecture' because the claims as well as the Specifications lack a definite description of a precise architecture to support the step actions in conjunction with the parallel construction (of registers) being inferred; and the 'parallel register architecture' thus recited will be treated as physical disposition/configuration (see Specifications Fig. 2) of registers in a way to facilitate the loading as recited in the configuration step.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. This rejection is based on the Practical Application Test requirement in regard to a claimed invention yielding of a result, as follows.

> The Federal Circuit has recently applied the practical application test in determining whether the claimed subject matter is statutory under 35 U.S.C. § 101. The practical application test requires that a " useful, concrete, and tangible result" be accomplished. An "abstract idea" when practically applied is eligible for a patent. As a consequence, an invention, which is eligible for patenting under 35 U.S.C. § 101, is in the "useful arts" when it is a machine, manufacture, process or composition of matter, which produces a concrete, tangible, and useful result. The test for practical application is thus to determine whether the claimed invention produces a "useful, concrete and tangible result".

Specifically, claim 1 recites a register spills handling method comprising rewriting spill instructions as a parallel register spill instruction based on some determination, and reconfiguring the spills back into a memory based on such rewriting via parallel register reloading. The whole operation is based on '**if** said register spill instructions can be associated' in the determination step, and as such, the IF condition and its implication do not reasonably convey the existence of any alternate action other than the IF-dependent *rewriting* action as recited. Thus, the crux of the method is based on some IF-determination or condition for otherwise the rewriting step would not actually take place. The claimed method cannot reasonably yield a steady result based on one condition which is perceived as a non-certainty; and amounts to a non-practical application, lacking sturdy support that a concrete, useful and tangible result is generated as a certainty at the end of the steps taken by the method. The claim is rejected for leading to a non-statutory subject matter.

Claims 2-7 do not reasonably convey alternate action taken in case a rewriting is not taken based on the IF clause requirement of the base claim; hence are also rejected for failing to fulfill the practical application test requirement as set forth above.

Claim 9 recites a system having a analyzing module, a rewriting module and a configuring module; all of which interacting with each other following the paradigm as set forth in claim 1; that is a rewriting step is performed based solely on the condition that 'said register spills instructions can be associated'. As such, the claimed system lacks reasonably teachings that a steady and certain result can be generated subsequent to the determination step being part of the analyzing module, the rationale of which being set forth above in claim 1. Besides, a system claim comprising solely of software modules without support of hardware entities to reasonably enable the realization of said modules' functionality would be considered non-statutory. As a whole, the claim exhibits the deficiency of uncertain possibility as to yield an action and a tangible result; and is rejected for leading to a non-statutory subject matter.

The claims 9-15 only recite further determining steps and configuring steps but fail to provide alternatives to the crucial rewriting step as set forth in the base claim, which does not cure to the uncertainty deficiency of the base claim. Claims 9-15 are also rejected for the same reasons as claims 2-7.

Likewise, claim 16 also exhibits the crucial rewriting step being dependent on a IF condition -- as in step (a); and along with claims 17-19 are rejected for not reasonably conveying that a certain result can be generated by the claimed system as a whole.

Claims 20-23 are rejected for leading to a non-statutory subject matter for the same reasons set forth in claims 16-19.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claims 1, 9, 16, 20 recite the phrase 'whether ... register spills instructions ... can be associated' (li. 3, li. 3, li. 3, li. 5 respectively). There is no sufficient support in the claim as to clarify or render more explicit the meaning of 'can be associated', i.e. a mutual correspondence set forth by the elements recited as 'register spills instructions' and the act recited as 'be associated', when the context required for a associating act entails at least 2 entities joined by an associating link. There is no clear definition in the Specifications as to what this 'can be associated' exactly signifies in terms of a mutual interaction (as in associated with something). One skill in the art would not be able to construe the 'can be associated' limitation in view of the above incomplete expression of an action; hence for the sake of examination, the indefiniteness of the above limitation will be treated as though the instructions are determined as to whether they can be reused or reloaded. Correction to the Specifications to clarify on such phraseology would be recommended.

9. Claims 7-8, 14-15, 18-19, 22-23 for reciting 'said memory stack' are rejected for lack of antecedent basis since the generic memory does not inherently include a stack; and the base claims does not recite a stack. This limitation will be treated as a separate stack or just a memory as set forth in the base claims.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kolson et al., 'A Method for Register Allocation to Loops in Multiple Register File Architectures', Proceedings of IPPP's 96, 1996, pp. 28-33 (hereinafter Kolson), further in view of Kahle et al, USPN: 5,867,684 (hereinafter Kahle).

As per claim 1, Kolson discloses a method of handling register spills, comprising:

determining whether register spill instructions in spill code generated by a register allocator can be associated (e.g. *require memory accesses when updated or necessary for computation* – pg. 28, R col.) and if said register spill instructions can be associated, then rewriting said register spill instructions (e.g. *must be loaded from memory* – Figure 4, pg. 31);

based on said rewritten register spill instruction, configuring storage of associated register spills in memory in such a manner that said register spills can be loaded back into said registers (Note: the update of register for runtime computation when variable are live and fetched from a memory discloses -by virtue of implicit teaching - a *load* back – see *must be loaded from memory* – Figure 4, pg. 31).

However, Kolson does not explicitly disclose that a parallel register architecture; nor does Kolson disclose rewriting spill instructions as a parallel register spill instruction or configuring memory spills by loading these into said parallel register in parallel. Kolson, however, discloses a architecture having multiple register implementation disposed as banks of General purpose registers and Auxiliary registers to support concurrent demand of load/store operations for a iterative loops such that a consolidated register file architectural approach

facilitates concurrent read and writes for live variables (see sec. 2, pg. 29: L col. Multiple Register Files; *performed in parallel* - sec. 3, L col.; *register banks* - sec: 6.1, Fig. 5, pg. 32). The concept of using a multiple register operation as suggested in parallel read/write in Kolson's register extension approach (see pg. 28, R col) is further disclosed by Kahle's architecture using multi-register for load/store operations (see Fig. 1-3; SUMMARY, col. 1-2 – Note: muli-register instruction reads on parallel register architecture instruction) to address pipeline or complex floating-point/iterative operations and to boost performance. Based on the structure of multiple banks of registers for concurrent operations in Kolson, it would have been obvious for one of ordinary skill in the art at the time the invention was made to apply a parallel register architecture instruction by Kahle to support the extended register banks as purported by Kolson for rewriting spill instructions as a parallel register instruction or loading spill instructions into said parallel register in parallel. One skill in the art --at the time where fast and complex architecture operating with extended words instruction sets exist -- would be motivated to do so because architecture as in Kahle's, equipped with specific instruction (multi-register instruction) making use of a parallel disposition of registers as suggested in Kolson's use of banks to effect one instruction operating on multiple registers as in Kahle's would further alleviate performance bandwidth and resources of runtime; and that would fit with Kolson's extended register endeavor (see Kolson: Abstract pg. 28; see Kahle: col. 1, lines 44-52).

As per claim 2, Kolson discloses wherein said parallel architecture comprises a primary register set and a secondary register set, and determining whether two register spill instructions can be paired (e.g. *General purpose registers and Auxiliary registers* - sec. 5.2, pg. 31; Fig. 5, pg. 32).

As per claim 3, Kolson discloses two register spill instructions are in a basic block within said spill code (see sec. 4.1, pg. 29-30).

As per claim 4, Kolson (in view of Kahle) discloses by virtue of claim 2 and the obviousness rationale in claim 1 (using multiple register in one load instruction) discloses determining whether said two register spill instructions relate to matching register locations in each of said primary register set and said secondary register set.

As per claim 5, Kolson (in view of Kahle) discloses determining whether any intervening instructions between said register spill instructions modify either of said register spill instructions (see *new_mapps, curr_maps* – Fig. 3, pg. 30; Fig. 4, pg. 31).

As per claim 6, Kolson does not explicitly disclose first allocating space on a memory stack to all paired register spills, then allocating space on said memory stack for any remaining register spills. But the use of memory stack in conjunction with variable loading and register allocation in view of spill code optimization was a known concept at the time the invention was made. It is well-known concept to use memory/register stack to provide for variables loading in context switch, complex iterations or nested procedure calls; hence based on the loop iteration and register consolidation by Kolson, it would have been obvious for one skill in the art to accommodate the loading instruction in a parallel register concurrent execution so that a register stack be used and spills code be loaded back according to the sequence needed; i.e. allocate first in stack register spills code in order as called for by the stack because this would enable the data needed for the procedure to be available in the correct sequence.

As per claim 7, Kolson does not disclose allocating space on said memory stack such that paired register spills are double word aligned; but based on at least a pair of registers (i.e.

multi-register or multiple word) simultaneously loaded as by Kahle's architecture (*lmw* – col. 4 ,lines 30-38) this *double-word* limitation would have been obvious in view of the rationale as set forth in claim 1.

As per claim 8, Kolson (in view of Kahle) discloses loading said paired register spills from said memory stack back into matching register locations in each of said primary register set and said secondary register set in parallel; but virtue of claim 2 and claim 1.

As per claim 9, Kolson (in view of Kahle) discloses a system for handling register spills in a parallel register architecture, comprising:

(a) a module for analyzing spill code generated by a register allocator to determine whether register spill instructions can be associated;

(b) a module for rewriting said register spill instructions as a parallel register spill instruction, if said register spill instructions can be associated;

(c) a module for configuring storage of associated register spills in memory in such a manner that said register spills can be loaded back into said registers in parallel based on said rewritten parallel register spill instruction;

the parallel register architecture, and the loading/rewriting to the parallel register as parallel register instructions having been addressed as obvious in view of Kahle in the rationale as set forth in claim 1.

As per claims 10-15, refer to claims 2, 4-8 for corresponding rejection as set forth therein respectively.

As per claim 16, Kolson (in view of Kahle) discloses a system for handling register spills in a parallel register architecture, comprising:

(a) means for determining whether register spill instructions in spill code generated by a register allocator can be associated;

(b) means for determining if said register spill instructions can be associated, then rewriting said register spill instructions as a parallel register spill instruction;

(c) means for configuring, based on said rewritten parallel register spill instruction, storage of associated register spills in memory in such a manner that said register spills can be loaded back into said registers in parallel;

the parallel register architecture, and the loading/rewriting to the parallel register as parallel register instructions having been addressed as obvious in view of Kahle in the rationale as set forth in claim 1.

As per claims 17-19, refer to claims 2, 7, 4 for corresponding rejection as set forth therein respectively.

As per claim 20, Kolson (in view of Kahle) a computer readable medium having computer readable program code embedded in the medium for handling register spills in a parallel register architecture, the computer readable program code including code for:

determining whether register spill instructions in spill code generated by a register allocator can be associated; for determining if said register spill instructions can be associated, then rewriting said register spill instructions as a parallel register spill instruction;

configuring, based on said rewritten parallel register spill instruction, storage of associated register spills in memory in such a manner that said register spills can be loaded back into said registers in parallel;

the parallel register architecture, and the loading/rewriting to said parallel register as parallel register instructions having been addressed as obvious in view of Kahle in the rationale as set forth in claim 1.

As per claims 21-23, refer to claims 2, 7, 4 for corresponding rejection as set forth therein respectively.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (272) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571)272-3756.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 (for non-official correspondence - please consult Examiner before using) or 571-273-8300 (for official correspondence) or redirected to customer service at 571-272-3609.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan A Vu
Patent Examiner,
Art Unit 2193
February 2, 2007